

CLAIMS

What is claimed is:

- 1 1. A content addressable memory (CAM) device comprising:
 - 2 a CAM array having a plurality of rows of CAM cells, each row including a
 - 3 plurality of row segments and being adapted to store a data word that spans a
 - 4 selectable number of the row segments;
 - 5 a priority index table coupled to the plurality of rows of CAM cells and adapted to
 - 6 store a plurality of priority numbers, each priority number being indicative of
 - 7 a priority of a corresponding data word stored in the CAM array.
- 1 2. The CAM device of claim 1 wherein the priority index table comprises a plurality
- 2 of storage rows, each storage row including a plurality of priority number storage
- 3 circuits that correspond to the plurality of row segments of a respective one of the
- 4 rows of CAM cells.
- 1 3. The CAM device of claim 2 further comprising a plurality of sets of match lines,
- 2 each set of match lines being coupled to the plurality of row segments of a
- 3 respective one of the rows of CAM cells and to the plurality of priority number
- 4 storage circuits of a respective one of the storage rows of the priority index table.
- 1 4. The CAM device of claim 3 wherein each row segment of the plurality of row
- 2 segments of each of the plurality of rows of CAM cells is adapted to compare a
- 3 comparand value to a value stored in the row segment and to activate a respective
- 4 one of the match lines if the value stored in the row segment matches the
- 5 comparand value.

1 5. The CAM device of claim 4 wherein the priority index table includes circuitry to
2 compare priority numbers stored within each of the plurality of priority number
3 storage circuits coupled to an activated match line.

1 6. The CAM device of claim 4 wherein each row segment of the plurality of row
2 segments is adapted to activate the respective one of the match lines by switching
3 off at least one transistor coupled between the respective one of the match lines and
4 a first reference voltage.

1 7. The CAM device of claim 2 wherein the priority index table further comprises
2 concatenation circuitry responsive to a configuration signal to concatenate
3 predetermined pairs of the priority number storage circuits such that each
4 concatenated pair of priority number storage circuits is enabled to store a priority
5 number that is larger than can be stored in a single priority number storage circuit.

1 8. The CAM device of claim 7 wherein the concatenation circuitry comprises a
2 plurality of switch circuits, each switch circuit being coupled between an output of
3 a first priority number storage circuit of a respective one of the predetermined pairs
4 of priority number storage circuits and an input of a second priority number storage
5 circuit of the one of the predetermined pairs of priority number storage circuits.

1 9. The CAM device of claim 8 wherein each switch circuit is adapted to switchably
2 couple the output of the first priority number storage circuit to the input of the
3 second priority number storage circuit if the control signal is in a first state.

1 10. The CAM device of claim 9 wherein each switch circuit comprises a transistor

2 having a control terminal coupled to receive the control signal, an input terminal
3 coupled to the output of the first priority number storage circuit and an output
4 terminal coupled to the input of the second priority number storage circuit.

1 11. The CAM device of claim 7 further comprising a concatenation control circuit to
2 generate the configuration signal in accordance with a configuration value.

1 12. The CAM device of claim 11 wherein the configuration value is indicative of a
2 selected number of the row segments.

1 13. The CAM device of claim 12 further comprising a configuration circuit to select the
2 selectable number of the row segments according to the configuration value.

1 14. The CAM device of claim 13 wherein the configuration circuit includes a
2 configuration storage to store the configuration value, the concatenation control
3 circuit being coupled to receive a signal indicative of the configuration value from
4 the configuration circuit.

1 15. The CAM device of claim 1 wherein at least one of the plurality of row segments
2 comprises a plurality of ternary CAM cells.

1 16. The CAM device of claim 1 further comprising a configuration circuit to select the
2 selectable number of the row segments according to a configuration value

1 17. The CAM device of claim 16 wherein the configuration circuit includes a
2 configuration storage to store the configuration value.

1 18. The CAM device of claim 17 wherein the configuration storage is adapted to store a
2 configuration value that specifies selection of between 1 and Z of the row segments,
3 Z being the number of row segments included within one of the plurality of rows of
4 CAM cells.

1 19. The CAM device of claim 18 further comprising a control circuit coupled to the
2 configuration circuit, and wherein the configuration circuit is responsive to a
3 control signal from the control circuit to store the configuration value in the
4 configuration storage.

1 20. The CAM device of claim 19 wherein the control circuit is responsive to an
2 instruction from an external device to output the control signal to the configuration
3 circuit.

1 21. The CAM device of claim 20 wherein the instruction includes an operand indicative
2 of the configuration value and wherein the control circuit outputs the control signal
3 in accordance with the operand to store the indicated configuration value in the
4 configuration storage.

1 22. The CAM device of claim 17 wherein the configuration storage comprises a non-
2 volatile memory to store the configuration value.

1 23. The CAM device of claim 1 further comprising a write circuit coupled to the
2 plurality of rows of CAM cells and adapted to output a data word to a selected row
3 of the plurality of rows of CAM cells, the data word having a size that spans a
4 number of the row segments in accordance with a configuration value.

1 24. The CAM device of claim 23 wherein the priority index table comprises a plurality
2 of storage rows, each storage row including a plurality of priority number storage
3 circuits that correspond to the plurality of row segments of a respective one of the
4 rows of CAM cells, and wherein the write circuit is further coupled to the plurality
5 of storage rows of the priority index table and is further adapted to store a priority
6 number that spans a number of the priority number storage circuits in accordance
7 with the configuration value.

1 25. The CAM device of claim 24 wherein, if the configuration value is a first value, the
2 write circuit is adapted to store a priority number that spans one of the priority
3 number storage circuits and wherein, if the configuration value is a second value,
4 the write circuit is adapted to store a priority number that spans two of the priority
5 number storage circuits.

1 26. The CAM device of claim 25 wherein the write circuit is adapted to store a priority
2 number that spans two of the priority number storage circuits by storing a priority
3 number that is stored in at least a portion of each of the two priority number storage
4 circuits.

1 27. The CAM device of claim 25 wherein, if the configuration value is the second
2 value, the write circuit is adapted to store a priority number that includes at least
3 one more bit than the number of bits that can be stored in a single priority number
4 storage circuit.

1 28. The CAM device of claim 1 wherein the priority index table is coupled to receive a

2 plurality of match signals from the CAM array during a compare operation, the
3 match signals indicating data words stored within the CAM array that match a
4 comparand value, the priority index table being further adapted to compare the
5 priority numbers that correspond to the data words indicated to match the
6 comparand value to identify a storage location within the CAM array of a highest
7 priority one of the data words indicated to match the comparand value.

1 29. The CAM device of claim 1 wherein the priority index table comprises a plurality

2 of priority number storage circuits arranged in rows and columns, each column of
3 priority number storage circuits corresponding to a respective column of row
4 segments within the CAM array.

1 30. The CAM device of claim 29 wherein each column of priority number storage

2 circuits is adapted to output a respective column priority number, the column
3 priority number having the highest priority of a selected set of priority numbers
4 stored in the column of priority number storage circuits.

1 31. The CAM device of claim 30 wherein each row segment of the plurality of row

2 segments of each of the plurality of rows of CAM cells is adapted to compare a
3 comparand value to a value stored in the row segment and to assert a match signal if
4 the comparand value matches the value stored in the row segment, the match signal
5 selecting a corresponding priority number within the priority index table to be
6 included within the selected set of priority numbers.

1 32. The CAM device of claim 30 further comprising a column priority logic circuit to

2 receive the column priority numbers from the respective columns of priority

3 number storage circuits, the column priority logic circuit being adapted to compare
4 the column priority numbers to determine a highest priority one of the column
5 priority numbers.

1 33. The CAM device of claim 32 wherein the column priority logic circuit includes
2 circuitry to generate a plurality of segment enable signals, each segment enable
3 signal corresponding to a respective column of the priority number storage circuits
4 and having an active state if a column priority number equal to the highest priority
5 one of the column priority numbers is output from the respective column of the
6 priority number storage circuits.

1 34. The CAM device of claim 32 wherein the column priority logic circuit is further
2 adapted to compare the column priority numbers to determine a highest priority pair
3 of the column priority numbers if a configuration signal is in a first state.

1 35. The CAM device of claim 34 wherein the column priority logic circuit includes
2 circuitry to generate a plurality of segment enable signals, each segment enable
3 signal corresponding to a respective column of the priority number storage circuits
4 and having an active state if the configuration signal is in the first state and if the
5 column priority number output from the respective column of the priority number
6 storage circuits is a component of the highest priority pair of the column priority
7 numbers.

1 36. The CAM device of claim 35 wherein the circuitry to generate a plurality of
2 segment enable signals is adapted to output, for each column of the priority number
3 storage circuits, a segment enable signal in the active state if the configuration

4 signal is in a second state and if a column priority number equal to the highest
5 priority one of the column priority numbers is output from the column of the
6 priority number storage circuits.

1 37. The CAM device of claim 36 further comprising enable circuitry to receive the
2 segment enable signals and the prioritized match signals, the enable circuitry being
3 adapted to generate at least one enabled match signal, the enabled match signal
4 indicating a prioritized match signal output by a column of priority number storage
5 circuits for which the corresponding segment enable signal is in the active state.

1 38. The CAM device of claim 33 wherein the columns of priority number storage
2 circuits are adapted to output a plurality of prioritized match signals, each
3 prioritized match signal indicating a priority number storage circuit having stored
4 therein the column priority number for a respective column of priority number
5 storage circuits.

1 39. The CAM device of claim 1 wherein the priority index table comprises a plurality
2 of priority number storage circuits, each priority number storage circuit including a
3 plurality of priority number storage cells, at least a portion of the priority number
4 storage cells within a predetermined subset of the priority number storage circuits
5 being responsive to a mode signal to operate in either a bypass mode or a compare
6 mode.

1 40. The CAM device of claim 39 further comprising a priority bit disable circuit to
2 generate the mode signal in accordance with a configuration value.

1 41. The CAM device of claim 1 further comprising a read circuit coupled to the
2 plurality of rows of CAM cells and adapted to read a data word from a selected row
3 of the plurality of rows of CAM cells, the data word having a size that spans a
4 number of the row segment in accordance with a configuration value.

1 42. The CAM device of claim 1 further comprising a match flag logic circuit coupled to
2 receive a plurality of match signals from the priority index table and to receive a
3 configuration signal that indicates the number of row segments within the selectable
4 number of row segments, the match flag logic circuit being adapted to logically
5 combine, according to the configuration signal, respective subsets of one or more of
6 the match signals to generate a match flag signal, the match flag signal indicating
7 whether the CAM array has a data word stored therein that matches a comparand
8 value.

1 43. The CAM device of claim 1 further comprising a multiple match flag logic circuit
2 coupled to receive a plurality of match signals from the priority index table and to
3 receive a configuration signal that indicates the number of row segments within the
4 selectable number of row segments, the match flag logic circuit being adapted to
5 logically combine, according to the configuration signal, respective subsets of one
6 or more of the match signals to generate a multiple match flag signal, the multiple
7 match flag logic signal indicating whether the CAM array has at least two data
8 words stored therein that match a comparand value and that correspond to priority
9 numbers stored within the priority index table that indicate the highest priority of all
10 match-enabled priority numbers stored within the priority index table.

1 44. The CAM device of claim 1 further comprising a priority encoder coupled to
2 receive a plurality of match signals from the priority index table and to receive a
3 configuration signal that indicates the number of row segments within the selectable
4 number of row segments, the priority encoder being adapted to generate, in
5 response to the match signals and in accordance with the configuration signal, an
6 address value that indicates a storage location within the CAM array of a data word
7 that matches a comparand value and that corresponds to a highest priority one of all
8 match-enabled priority numbers stored within the priority index table.

1 45. A method of operation within a content addressable memory (CAM) device, the
2 method comprising:
3 storing a data word in a CAM array of the CAM device, the data word spanning a
4 number of CAM cells within the CAM array in accordance with a first
5 configuration value; and
6 storing a priority number in a priority index table of the CAM device, the priority
7 number indicating a priority of the data word relative to other data words
8 stored in the CAM array.

1 46. The method of claim 45 wherein storing a priority number within the priority index
2 table comprises storing a priority number that spans a number of storage elements
3 within the priority index table according to the first configuration value.

1 47. The method of claim 45 further comprising:
2 receiving the first configuration value; and
3 storing the first configuration value within the CAM device.

1 48. The method of claim 47 wherein storing the first configuration value within the
2 CAM device comprises storing the first configuration value in a configuration
3 storage circuit within the CAM device.

1 49. The method of claim 45 wherein storing a priority number within the priority index
2 table comprises storing a priority number that spans a number of storage elements
3 within the priority index table according to a second configuration value.

1 50. A method of operation within a content addressable memory (CAM) device, the
2 method comprising:
3 comparing a comparand value to a plurality of data words stored within a CAM
4 array to identify data words that, at least in part, match the comparand value;
5 selecting a plurality of priority numbers according to the identified data words, each
6 of the priority numbers having a constituent number of bits according to a first
7 configuration value; and
8 comparing the plurality of priority numbers to determine a highest priority one of
9 the identified data words.

1 51. The method of claim 50 wherein each of the plurality of data words has a
2 constituent number of bits according to the first configuration value.

1 52. The method of claim 51 wherein the CAM array includes a plurality of rows of
2 CAM cells, each row including a plurality of row segments, and wherein the first
3 configuration value indicates a number of row segments spanned by each of the
4 plurality of data words.

1 53. The method of claim 52 wherein the number of constituent bits of each of the
2 priority numbers corresponds to the number of row segments spanned by each of
3 the plurality of data words.

1 54. The method of claim 50 wherein the first configuration value indicates an operating
2 mode for the CAM device, the priority numbers having a constituent number of bits
3 determined in part by the operating mode.

1 55. The method of claim 50 wherein the first configuration value indicates an operating
2 mode for the CAM device and a word size of the plurality of data words, the
3 priority numbers having a constituent number of bits that is determined by the
4 operating mode and the word size.

1 56. The method of claim 55 wherein the priority numbers have a number of constituent
2 bits in logarithmic proportion to the word size when the first configuration value
3 indicates a forwarding mode of operation for the CAM device.

1 57. The method of claim 50 wherein comparing the plurality of priority numbers to
2 determine a highest priority one of the identified data words comprises comparing
3 the plurality of priority numbers in a first comparison operation if the first
4 configuration value indicates that the plurality of priority numbers have a first
5 number of constituent bits, and comparing the plurality of priority numbers in a
6 second comparison operation if the first configuration value indicates that the
7 plurality of priority number have a second number of constituent bits.

1 58. A system comprising:

2 a CAM device having a CAM array and a priority index table; and
3 a processor coupled to output configuration information to the CAM device, the
4 configuration information indicating a width of data words to be stored in the
5 CAM array and a width of priority numbers to be stored in the priority index
6 table.

1 59. The system of claim 58 wherein the CAM device includes a configuration storage
2 circuit to store the configuration information.

1 60. The system of claim 58 wherein the processor is a network processor.

1 61. The system of claim 58 wherein the CAM array includes a plurality of rows of
2 CAM cells, each row including a plurality of row segments, and wherein the
3 configuration information indicates a number of row segments spanned by data
4 words to be stored in the CAM array.

1 62. The system of claim 58 wherein the CAM device is implemented in a first
2 integrated circuit and the processor is implemented in a second integrated circuit.

1 63. The system of claim 58 wherein the first integrated circuit and the second integrated
2 circuit are packaged in a single integrated circuit package.

1 64. The system of claim 63 wherein the CAM device and the processor are
2 implemented in a single integrated circuit.

1 65. A method of controlling a content addressable memory (CAM) device, the method
2 comprising:

3 outputting first configuration information to the CAM device, the first configuration
4 information indicating a width of data words to be stored in a first CAM array
5 within the CAM device and a width of priority numbers to be stored in a first
6 priority table within the CAM device;
7 outputting at least one write instruction to the CAM device to instruct the CAM
8 device to store a data word within a data storage field of the first CAM array,
9 the data storage field including a number of CAM cells according to the
10 configuration information, and to instruct the CAM device to store a priority
11 number within a priority number storage field of the first priority table, the
12 priority number storage field including a number of priority storage cells in
13 accordance with the configuration information.

1 66. The method of claim 65 wherein the first configuration information further
2 indicates either a first operating mode or a second operating mode of the CAM
3 device, the CAM device including circuitry to decode the priority number into a
4 mask word and store the mask word within a mask storage field of the first CAM
5 array if the configuration information indicates the first operating mode.

1 67. The method of claim 65 further comprising outputting second configuration
2 information to the CAM device, the second configuration information indicating a
3 width of data words to be stored in a second CAM array within the CAM device
4 and a width of priority numbers to be stored in a second priority table within the
5 CAM device.

1 68. The method of claim 67 further comprising outputting third configuration
2 information to the CAM device, the third configuration information indicating a

3 relative priority between data words stored within the first CAM array and data
4 words stored within the second CAM array.

1 69. The method of claim 67 further comprising outputting a compare instruction to the
2 CAM device, the compare instruction including a class code, the CAM device being
3 responsive to the compare instruction to select, according to the class code, at least
4 one of the first and second CAM arrays to participate in a compare operation.

1 70. A content addressable memory (CAM) device comprising:
2 a CAM array having a plurality of CAM cells;
3 means for writing a data word into the CAM array, the data word spanning a
4 number of the CAM cells within the CAM array in accordance with a first
5 configuration value;
6 a priority index table coupled to the CAM array; and
7 means for writing a priority number into the priority index table, the priority
8 number indicating a priority of the data word relative to other data words
9 stored in the CAM array.

1 71. The CAM device of claim 70 wherein the means for storing the priority number
2 comprises means for storing a priority number that spans a number of storage
3 elements within the priority index table according to the first configuration value.

1 72. The CAM device of claim 70 further comprising:
2 means for receiving the first configuration value; and
3 means for storing the first configuration value within the CAM device.

1 73. The CAM device of claim 70 further comprising means for comparing priority
2 numbers stored within the priority index table.

1 74. The CAM device of claim 70 further comprising means for reading a data word
2 from the CAM array.

1 75. The CAM device of claim 70 further comprising:
2 means for comparing data words stored within the CAM array with a comparand
3 value; and
4 means for generating a match flag signal that indicates whether at least one of the
5 data words stored within the CAM array matches a comparand value.

1 76. The CAM device of claim 75 further comprising means for generating a multiple
2 match flag signal that indicates whether two or more of the data words stored within
3 the CAM array match the comparand value and correspond to respective priority
4 numbers stored within the priority index table that are equal to a highest priority
5 one of all match-enabled priority numbers stored within the priority index table.

1 77. The CAM device of claim 70 further comprising means for generating an address
2 value that indicates a storage location within the CAM array of a data word that
3 matches a comparand value and that corresponds to a highest priority one of all
4 match-enabled priority numbers stored within the priority index table.

1 78. The CAM device of claim 70 further comprising means for selectively writing, into
2 the priority index table, a priority number that spans more than one priority number
3 storage circuit within the priority index table.

1 79. A content addressable memory (CAM) device comprising:
2 a CAM array to store a plurality of data words;
3 means for identifying data words stored within the CAM array that, at least in part,
4 match a comparand value;
5 a priority index table to store priority numbers;
6 means for selecting priority numbers stored within the priority index table
7 according to the identified data words, each of the selected priority numbers
8 having a constituent number of bits according to a configuration value; and
9 means for comparing the selected priority numbers to determine a highest priority
10 one of the identified data words.

1 80. The CAM device of claim 79 wherein each of the plurality of data words has a
2 constituent number of bits according to the configuration value.

1 81. The CAM device of claim 79 wherein the means for comparing the selected priority
2 numbers to determine a highest priority one of the identified data words comprises
3 means for comparing the selected priority numbers in a first comparison operation
4 if the configuration value indicates that the selected priority numbers have a first
5 number of constituent bits and means for comparing the selected priority numbers
6 in a second comparison operation if the configuration value indicates that the
7 selected priority numbers have a second number of constituent bits.